REMARKS/ARGUMENTS

Claims 1-32 are pending in the present application.

This Amendment is in response to the Final Office Action mailed March 5, 2003. In the Final Office Action, the Examiner rejected claims 1-2, 14-15, 27-28 under 35 U.S.C. §102(e); and claims 3-13, 16-26, 29-32 under 35 U.S.C. §103(a). Applicant has amended claims 1, 14, and 27. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 102

1. In the Final Office Action, the Examiner rejected claims 1-2, 14-15, and 27-28 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,237,064 issued to Kumar et al. ("Kumar"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of anticipation.

Applicant reiterates the arguments set forth in the previously filed Response to the Office Action. In particular, Applicant contends that Kumar does not disclose, either expressly or inherently, the chipset cache being located in a memory controller. Kumar merely discloses a L2 data array coupled to the processor core by a backside bus. The memory controller is coupled to the bus controller over the frontside bus (Kumar, col. 3, lines 14-17). The data array therefore is not located in the memory controller. To clarify the claim language, claims 1, 14, and 27 have been amended.

To anticipate a claim, the reference must teach every element of a the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989).

Therefore, Applicant believes that newly amended independent claims 1, 14, 27 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejection under 35 U.S.C. §102(e) be withdrawn.

Rejection Under 35 U.S.C. § 103

1. In the Final Office Action, the Examiner rejected claims 3-13, 16-26, and 29-32 under 35 U.S.C. §103(a) as being unpatentable over Kumar in view of U.S. Patent No. 6,438,657 issued to Gilda ("Gilda"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness.

Applicant reiterates the arguments set forth in the previously filed Response to the Office Action.

There is no motivation to combine Kumar and Gilda because neither of them addresses the problem of controlling cache memory in external chipset. There is no teaching or suggestion that an external cache is located in a memory controller is present. Kumar, read as a whole, does not suggest the desirability of controlling an external cache in a memory controller from the processor. Kumar and Gilda, taken alone or in any combination, does not disclose, suggest, or render obvious a chipset cache controller to control a chipset cache located in a memory controller. The Examiner failed to establish a prima facie case of obviousness and failed to show there is teaching, suggestion or motivation to combine the references. "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight

knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re ROUFFET, 149 F.3d 1350 (Fed. Cir. 1996), 47 USPQ 2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

In the present invention, the cited references do not expressly or implicitly suggest controlling an external cache in a memory controller using a processor. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Kumar and Gilda is an obvious application of cache control using a processor.

Therefore, Applicant believes that independent claims 1, 14, 27 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. §102(e), and 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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